MAGNETORESISTIVE READ ACCESS MEMORY - An Analysis of MRAM Market

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Executive Summary

Magnetoresistive memory (MRAM) is one of the forerunners of the nanotechnology memories lined to replace the traditional memories like Flash, DRAM and SRAM. It stores data using magnetic charge as compared to electrical charge. Other competing nanotech memories include Ferroelectric RAM (FRAM), Phase change RAM (PRAM), holographic and nanocrystalline memories. All these next generation technologies are attempts to develop the "perfect" memory. While none of them succeeds in all areas, all of them make key advancements in at least some of the important memory characteristics.

MRAM promises the density of DRAM with the speed of SRAM and data integrity of Flash – together resulting into instant on non volatile computers and tiny, super fast and reliable portable devices. It promises a high-capacity next-generation memory that can replace SRAM/Flash combos and battery-backed up RAM as well as supplying improved non-volatile memory solutions for high-end mobile products. Freescale has recently started volume production on 4 Mbit MRAM and there are as many as 20 firms actively pursuing this opportunity. Meanwhile, important firms such as Intel, Freescale, Micron, Samsung, STMicroelectronics are beginning to settle on new technology platforms for the post-Flash era and are finding ovonic/PRAM and nanocrystalline memories increasingly to their liking.

It is estimated that nanotechnology enabled memories will be a 7 B$ market in 2010, a time when traditional memories are predicted to reach their limit. MRAM's share in this market is estimated to be 1.5 B$. Getting the cost structure and the volumes for MRAMs to the point where it can have a huge impact on giant markets is still a challenge.

Technology Assessment

MRAM is one of several memory innovations aiming to replace DRAM and nonvolatile flash memory. It is claimed to offer something close to the speed of SRAM, with a density approaching that of single-transistor DRAM and the ability to store information when power is removed, like flash memory or EEPROM. Memories based on MRAM have been seen to be in a race to develop a 'universal memory' that could replace SRAM, DRAM and flash in many applications.

Unlike conventional RAM chip technologies, data is stored as magnetic storage elements instead of electric charge or current flow. The elements are formed from two magnetic plates, each of which can hold a magnetic field, separated by a thin insulating layer. One of the two plates is a permanent magnet set to a particular polarity; the other's field will change to match that of an external field. A memory device is built from a grid of such "cells".

Data is written to the cells by creating an induced magnetic field in a grid of write lines above and below the cells. To write to a particular cell, one X and one Y write line is charged, and a transistor lying on one of the two lines switches the current on at that point. The resulting current creates a magnetic field, which flips the polarity of the "writable" plate to match the induced field. To improve speed, writing is done in parallel by holding one X (or Y) line "high" and then powering all the Y lines along that row that need to be flipped.

For Reading, the controlling transistor is "switched on", and the resulting current in the read line is sensed. Due to the magnetic tunnel effect, the electrical resistance of the insulator between the plates is changed by the magnetic field being held in the two plates in the cell. By measuring the resulting current output, the resistance inside any particular cell can be determined, and from this the polarity of the writable plate. Typically if the two plates have the same polarity this is considered to mean "0", while if the two plates are of opposite polarity the resistance will be higher and this means "1".

A newer technique, spin-torque-transfer, uses spin-aligned ("polarized") electrons to create the magnetic field. This lowers the amount of current needed to write the cells, making it about the same as the read process. Here the memory is built of units called Magnetic Tunnel Junction (MTJ) which consist of two ultra thin magnetic metal layers separated by an insulator. Within a single magnetic layer, all the electrons 'spins are aligned. An electric current will have an easier time passing through the layers if the spins of the two magnetic layers are aligned parallel to each other. They will resist current if their spins are anti parallel; this resistance is called magnetoresistance. Layers with parallel spin may represent 0 and anti parallel as 1. Each MTJ is a memory cell and stores a single bit of data where data can be read as a measure of the magnetoresistance. To write data into the cell, one needs to apply a magnetic field to flip the spin orientation of one of the layers. Reading is accomplished by sensing a change in the resistance.

There are two types of cell flavors for MRAMs -- FET and cross point.

Competing nanomemory technologies

Till date, ***Ferro Electric RAM (FRAM)*** is the best bet in the nanotechnology memory space in terms of commercial potential coming ahead of MRAM. FRAMs have been researched by Celis Semiconductor, Hynix, Macronix, Infineon, Ramtron, Samsung, Sanyo, Texas Instruments and Toshiba. Ramtron is a major player. It has FRAM chips in mass production with the bulk of its shipments being direct replacements for use in data acquisition devices, such as meters, that now use SRAMs equipped with battery backup. TI has licensed FRAM from Ramtron and is working along with it. It had planned a 90 nm FRAM process ready in 2005 but then stepped back to a 130 nm process. FRAM is very competitive in the low power embedded space and is also logic library compatible. TI plans to use FRAM for chipsets after making the discrete parts.

Technologically similar to writeable DVDs, ***Phase Change Memories (PRAM)*** are probably just behind MRAM. PRAM is also called ovonic or chalcogenide memory. Elpida Memory, Intel, Philips Research, Samsung and STMicroelectronics are amongst the few players who have worked in PRAM technologies. Much of the basic IP for ovonic memory is owned by a firm called Ovonyx in which Intel has invested undisclosed amounts, So far, PRAM yields and reliability have been low compared with FRAMs and MRAMs; but with the giant R&D budgets at Samsung, Intel and Philips targeting the problem, solutions will likely be found. Samsung has already demonstrated a "differential" PRAM architecture that ups reliability. Macronix International Co. Ltd., in Taiwan, has also shown both PRAMs and related resistive RAMs (RRAMs), while Infineon has shown experimental organic RRAMs. It is felt that the single most important factor in the rise of ovonic memory has been its adoption by Intel as its favored replacement for Flash; this has given this technology credibility.

Nanocrystalline memory uses tiny silicon crystals to store data. Freescale and Micron back this technology. Freescale Semiconductor says replacing floating polysilicon gates with nanocrystalline silicon will cut chip size and mask steps, significantly reducing the cost of its embedded flash memory products, starting with the 65nm node in 2008-2009. The company has demonstrated a 24Mbit memory array made with 90nm process technology, using gates made of a monolayer of nanocrystals of silicon, encapsulated in a dielectric oxide.

Holographic memory is a technique that can store information at high density inside crystals or photopolymers. As current storage techniques such as DVD reach the upper limit of possible data density (due to the diffraction limited size of the writing beams), holographic storage has the potential to become the next generation of storage media. The advantage of this type of data storage is that the volume of the recording media is used instead of just the surface. Some of the key players in this sector are InPhase Technologies of the US (originally founded as a Lucent Technologies venture in 200), Optware Co Ltd of Japan , Sony Corp of Japan, Samsung Advanced Institute of Technology of Korea, Thomson of France, Philips Research of the Netherlands and Daewoo Electronics Corp of Korea. Holographic memory is likely to be a prime contender for both high-end data storage and consumer video media markets in the not-too-distant-future

Potential Applications

- Cell phones, PDAs and notebooks:
  MRAM is an attractive alternative to deploying both Flash and DRAM. It can save money and space. With software applications residing in memory, mobile devices will rapidly power up to exactly where they were when they were turned off. This will prove useful for someone who wants to use his notebook for a few minutes between flights.
- Computing and networking:
  MRAM can be used to avoid boot-up delays and to provide faster access to hard drives and non- volatile backup capabilities. At present, BIOS tends to use high cost, low density EEPROM or battery backed-up SRAM and volatile memory is used to alleviate I/O bottlenecks. In such applications, MRAM could prove in economical.
- Factory automation:
  Microcontrollers and robots typically employ both RAM and PROMs/Flash. Lower costs will be achieved by replacing these two chips with one MRAM device.
- RFID:
  RFID tags need low- cost, non-volatile memory and at least one company (Micromem Technologies) is targeting this sector with MRAM products. A price point that makes MRAM economically viable for RFID applications will almost certainly push MRAM into other cost-sensitive areas.
- Military:
  MRAM is "rad hard" which makes it suitable for use in missiles and spacecraft and perhaps on battlefields where equipment could potentially be exposed to tactical nuclear weapons. Honeywell is already selling products for this sector.
- Sensors, smart cards
- Portable recording and playback devices
- Cell phones and other handhelds
- Mobile computing

Major Players

IBM and Infineon

IBM research pioneered the development of tiny, thin film magnetic structures as early as 1974. It developed the magnetic tunnel junction (MTJ), the technology at the heart of MRAM.

IBM teamed up with Infineon Technologies Corporation for a 200-mm-wafer-scale technology development in 0.18 micron CMOS in a joint effort known as the MRAM Development Alliance (MDA). The mission of the MDA was to develop a competitive and scalable MRAM technology. In June 2003, IBM and Infineon Technologies announced that they had developed the most advanced MRAM technology to date by integrating magnetic memory components into a high-performance logic base. They presented a high-speed 128Kbit MRAM core fabricated with a 0.18 micron logic-based process technology. The MRAM cells were 1.4 square microns in area and had cross-point architecture.

The MDA work spanned a period of three and a half years from late 2000 to mid-2004. One of the final activities of the MDA was the transfer of the MRAM technology into a manufacturing site, the jointly IBM–Infineon-owned Altis Semiconductor Corporation in France. Following the end of the MRAM Development Alliance in mid-2004, Infineon continued its MRAM development activity at the Altis site. After the transfer to Altis, IBM refocused its MRAM effort into a more exploratory program comprising a basic yield demonstration component for 0.18 micron technology development; consistent with the desired IBM product vision for MRAM as an embedded memory at an advanced CMOS node.

Infineon unveiled a 16-Mbit prototype based on 0.18 micron technology in June 2004. It is also looking at other memory technologies, especially phase-change RAM (PRAM) and conductive-bridging RAM (CB-RAM).

Freescale

Freescale's MRAM technology differs from the original IBM version in having FET architecture i.e. it has a FET controlling each bit cell. This technology is presently called 1T-1MTJ technology. Each bit cell has one transistor and magnetic tunnel junction.

Freescale has patented its own piece of IP called Savtchenko bit cell which allows greater control and a reduction in accidental spin flips when writing data with magnetic fields.

In mid 2002, Freescale Semiconductor successfully demonstrated a 1 Mb non volatile, low-power MRAM chip with read and write cycles of less than 50 ns. It started sampling 4 Mbit nonvolatile memories made using 0.18u manufacturing process to a limited number of customers in Oct 2003. This came in 2 versions: one with 35ns access time and other 25 ns. Both needed 3.3V power supply.
Then in 2004, it cast its 4 Mbit MRAM as a standard product.

In June 2006 in Japan, Freescale demonstrated a 90nm MRAM with an aluminum oxide tunneling layer. The demo showed that the 180nm cell could be shrunk to

2.9^2 in a 90nm logic process, which includes low-k dielectrics. Now, Freescale is replacing aluminum oxide with magnesium which will reportedly improve the bit resistance and allow the tunneling layer to be thinned slightly. With aluminum oxide in the magnetic tunnel junction, MRAMs undergo a 30 percent resistance change as the bit changes from zero to one. With magnesium oxide, that resistance change can be 90 percent to 100 percent, with huge implications for MRAM technology.

Just recently, on 10th July 2006, Freescale announced that it has moved MRAM into volume production. The first device, MR2A16A, is a 4Mbit product and is suitable for use in cache buffers and configuration storage memories. It works in the commercial temperature range and is a 3.3V device featuring 35ns read and write cycle times.

TSMC and ERSO / ITRI

Taiwan Semiconductor Manufacturing Co. Ltd. (TSMC) and the Electronic Research and Service Organization (ERSO) of ITRI, Taiwan announced the joint R&D project on MRAM technology in March 2002.

In one paper at IEDM in December 2004, TSMC, ERSO and others provided more details about their collective efforts in MRAM technology. TSMC claimed to have developed novel MRAM structures based on a 0.18-micron process and a pillar write word line (PWWL) cell. The company proposed to shrink the bit size while reducing the writing current by a factor of two, according to the paper.

Ming-Jinn Tsai, director of the nanoelectronics technology division at ERSO, mentioned early this year that MRAM has a niche market in the future and that ERSO and TSMC will be moving into pilot production stage very soon.

Renesas and Mitsubishi

Renesas Technology and Mitsubishi Electric Corp. have been doing a joint research on MRAM technology. They also use the 1T-1MTJ architecture, allowing very high speeds (possible operating speeds claimed to be in excess of 143 MHz) as compared to cross point architecture. In Dec 2004 at IEDM, Renesas announced that it has developed a high speed, high reliability MRAM technology for SoC use and that using this technology, it has fabricated a prototype 1 Mbit MRAM in 0.13 micron CMOS process.

By studying the relationship between the magnetoresistance (MR) ratio and resistance area (RA) in the MTJ, the joint development team applied correlativity with read speed and established an original method of finding the optimal conditions for achieving high speed.

Their main innovation is the use of CoFeB (ferrocobalt boron) as a magnetic material, giving better results than with the CoFe used previously in Renesas MRAM. Using these developments, it's possible to achieve data read times of 5.2ns, making the read cycle approximately 7ns. Furthermore, an experiment of 1 trillion write cycles at elevated temperatures (>150 deg C) showed almost no degradation. The MRAM is fabricated in 0.13 micron technology using 4-layer copper wiring and, Renesas claims, it's the world's smallest memory cell at 0.81 square microns

In Dec 05, Renesas and Grandis announced to collaborate a development of 65 nm MRAM employing spin torque transfer and that Renesas Technology will start to ship microcomputers and SoC products incorporating 65 nm process STT-RAM(TM) in the near future.

Renesas is also doing a feasibility study of embedding MRAM and PRAM into microcontrollers and developing them jointly with Hitachi and Mitsubishi Electric, both parent companies of Renesas. The new memory technology will be available around 2010, along with improvement of existing technologies and innovative development.

Toshiba and NEC

At the IEDM in late 2004, Toshiba, working in partnership with NEC, announced its new cell architecture based on a cross-point cell. The architecture is a kind of hybrid with four cross point (CP) cells controlled by each transistor.

Toshiba said that the new cell architecture realizes a CP cell with fast read times; typical read time of 250ns being still four times faster than conventional CP cells, and the cells being of the same size as conventional DRAM and CP MRAM.

Toshiba and NEC also pioneered a new shape for the MTJ; a rectangle with arc shaped bulges on either side with which they halved the write current compared to previous technology and reduced write errors. The prototype is a 1Mbit chip fabricated using 130nm process technology; it operates on 1.5V.

In Feb 2006, Toshiba and NEC announced that the development of an MRAM which combined high density with the fast read and write speed. The new MRAM achieved a 16-megabit density and a read and write speed of 200-megabytes a second, and a low voltage operation of 1.8V.

Till date, a major challenge of MRAM development has been the acceleration of read speeds: the current drive circuit used to generate the magnetic field for writing degrades read operation from memory cells. The circuit design of the new MRAM developed by Toshiba and NEC divides the current paths for reading and writing, thus realizing a faster read speed. It also reduces equivalent resistance in wiring by approximately 38% by forking the write current. These innovations together achieve a read and write speed of 200-megabytes a second and a cycle time of 34 nanoseconds — both being claimed as the world's best performance for MRAM. This performance is underlined by a low operating voltage of only 1.8V. In addition, the overall circuit design has also been optimized achieving a chip that, at 78.7mm2, is approximately 30% smaller than its equivalent without the new circuit design. The new MRAM is said to be the worlds smallest in the 16-megabit era.

The main specs include .13u nm CMOS process, 0.24 u MRAM, 16 megabits with cell size of 1.872 sq microns, cycle time of 34 ns, read/write speed of 200 megabytes/sec and powered by 1.8v.

Development of these new MRAM technologies was supported by grants from Japan's New Energy and Industrial Technology Development Organization (NEDO).
Full details of the new technology were presented on February 6 2006 at ISSCC (International Solid-State Circuits Conference) 2006 in San Francisco, USA.

Toshiba Corp. and NEC Corp. announced in June 2006 the joint development of the key technology required for expanding the capacity of MRAM to the level of 256 Mbit. The key technology is mainly composed of three elemental technologies: First is a technology to prevent erroneous writing, which is enabled by optimizing the shape and structure of the TMR device. The two companies have developed a propeller-shaped TMR device to improve the writing control. The second technology achieves high-speed writing while maintaining the low-voltage operation at the same time, which is made possible through the improvement of the wiring configuration and optimization of the current drive. Third includes a variety of process technologies that are required in the microfabrication of the MRAM, such as etching techniques for processing magnetic materials.

The two companies have prototyped a 16 Mbit product employing the above elemental technologies. The prototyped chip has reportedly been confirmed for operation in simulations even with memory capacity expanded to 256 Mbit. Further, the chip boasts the industry's lowest write current of approximately 4 mA. It features the cycle time of 34 ns, the read/write data rate of 200 MB per second and the supply voltage of 1.8 V. 240 nm and 130 nm generations for the MRAM device and peripheral logic circuits technologies, respectively, were adopted in manufacturing the chip.

Cypress

Cypress Semiconductor was one of licensee of the MRAM technology from NVE Corporation. However it sold its MRAM business (Silicon Magnetic Systems, its subsidiary founded to commercialize MRAMs) in early 2005 after successfully sampling a 256Kbit device. The sampled MRAM was the three transistor, two magnetic tunneling junction (3T-2MTJ). It also demonstrated 256-kilobit MRAMs working in customers' systems. Its CEO Rodgers commented that they no longer believed that 1T-1MTJ MRAM technology could successfully attack the SRAM market, leaving MRAM as a niche technology with higher bit pricing than SRAM.

Cypress 'strategy was to commercialize their MRAM technology first in the niche, battery-backup SRAM markets, and then to grow by adding to their product portfolio a family of high density MRAMs ranging from 4 to 64 megabits in density.

NVE Corp

Minnesota based NVE Corp. had been developing spintronic based MRAM since 1989 working mainly on government research grants and building up an impressive IP portfolio in the process including the basic patents required for a wide range of commercial MRAM applications.

NVE and Cypress entered into a technology exchange agreement in 2002. In return for access to NVE's IP and 17% equity stake, Cypress invested 6.2 MUSD in the company and agreed to manufacture a minimum of 500 wafers per quarter that NVE could package and sell under their own label. Cypress sold all its shares in NVE in September 2003 – the same day when it announced delays in MRAM development, thus raising a lot of speculations.

NVE Corp, which in the past had been pushing both IP and standard products for MRAM market, revised its strategy and announced in April 2005 that it was moving towards an IP model. It said that it would now sell only its intellectual property for a 256-kbit MRAM design. The statement included that NVE is well positioned with critical intellectual property covering a broad range of near term and long term MRAM designs. Hence NVE's MRAM strategy would be to focus on the IP business model providing the technology to enable memory design rather than both providing technology and selling devices. This was announced after Cypress announced about discontinuing its efforts in the MRAM products.

Honeywell

Honeywell started MRAM development in Sep 2003 and redirected its efforts to radiation hardened 1M MRAM based on Honeywell SOI and Motorola MTJ MRAM technology. It licensed Motorola MRAM technology for its aerospace and military applications a month later.

In June 05, it posted a data sheet for a 1-Mbit radiation-hard magnetic RAM to its website in the form of a "pdf" file. While the specification sheet was labeled as advanced information, a source said the Honeywell memory was neither a prototype nor sample but a commercial product.

The Honeywell 1-Mbit MRAM, organized as 64K by 16-bits, is fabricated in Honeywell's radiation-hardened 150-nanometer silicon-on-insulator manufacturing process technology, and is designed for use in low-voltage systems operating in radiation environments. The MRAM operates over the full military temperature range and is operated with 3.3-V and 1.8-V power supplies, according to the specification sheet.

In Aug 2005, Silicon Laude announced the world's first radiation hardened and radiation tolerant MCS8051 instruction capable microcontrollers that could directly interface with Honeywell's HXNV-0100 64kx16 radiation hardened MRAM.

Market Analysis

A. Market Outlook

In the age of nanotechnology, all bets are off on the innovative staying innovative for long. The new memory technologies will not begin to displace old fashioned DRAM and Flash until they can compete on price, and it will take billions of dollars of research and development spending to get to that point. Micro and Nanotechnology analysis company, NanoMarkets, predicts that by 2010, four key segments will have emerged in the nano-enabled memory markets: MRAM, Ovonic, Holographic and Nanocrystalline. It projects that MRAM will account for $1.5 billion in revenues in 2010 followed by holographic and nanocrystalline at $980 million each and ovonic memory at $877 million. Intel Corp. sees current flash memory technology sustaining until the end of the decade, pushing out the need for "universal memory" until 2010.

MRAM promises a high-capacity next-generation memory that can replace SRAM/Flash combos and battery-backed up RAM as well as supplying improved non-volatile memory solutions for high-end mobile products. MRAM is already sampling, Freescale has just recently moved MRAM into volume production and there are as many as 20 firms actively pursuing this opportunity. Meanwhile, important firms such as Intel, Freescale, Micron, Samsung, STMicroelectronics are beginning to settle on new technology platforms for the post-Flash era and are finding ovonic and nanocrystalline memories increasingly to their liking. Holographic memory is likely to be a prime contender for both high-end data storage and consumer video media markets in the not-too-distant-future.

Nanomemory has made a slow start with several promised product launches that have failed to materialize. Nonetheless 2010 is seen as a breakout year for nanomemory, because by that time conventional solutions will simply be unable to scale further or provide the memory requirements needed for ubiquitous computing. Technical improvements and real commitments from larger firms to specific nanomemory platforms have now brought nanomemory much closer to reality.

B. What is driving the market?

The main reason for growing commitments is that scaling has now become a serious issue for the memory industry. Leakage is a major hurdle at 65 nm and beyond. 3D structures offer one solution, but there's a limit on how far one can go in this. Similarly, SRAM makers have largely abandoned large 6T cells in portable devices in favor of 1T pseudo SRAM (PSRAM). But again, this is only a holding action until something better comes along. Flash has a serious architectural scaling problem that seems likely to become critical well below 90 nm.

Such problems are making both semiconductor firms and OEMs take nanomemories much more seriously. Not only are many of these new technologies inherently more scalable, but they seem well suited to the next

generation of mobile computing and communications that will demand high capacity memories capable of storing and rapidly accessing video and large databases without overburdening battery power sources.

In light of such issues, Nanomemory solutions seem to be a key technology. FRAM (ferroelectric-RAM), MRAM (magnetic-RAM), and other next generation technologies are all attempts to develop the "perfect" memory: One that is nonvolatile, whose bits can be fully altered, with ultra fast read and write rates and an infinite number of rewrite cycles. None of them succeeds in all areas, but all of them make key advancements in at least some of these important memory characteristics.

The advantages of storing information through magnetic resistance instead of electrical charge are many. The first one is non volatility i.e. magnetic memories retain data which doesn t need to be refreshed frequently unlike the traditional ones which require a constant flow of electric charge. In addition, these magnetic memories require less power which is becoming a major issue in the Deep Sub Micron designs.

Amongst the nanotechnology memories, MRAM promises the density of DRAM with the speed of SRAM and data integrity of Flash – together resulting into instant on non volatile computers and tiny, super fast and reliable portable devices. In a comparison study of MRAM with traditional memories, in general MRAM proponents expect much lower power consumption (up to 99% less) compared to DRAM. Compared to Flash memory, Flash and MRAM are very similar in power requirements while reading. However, Flash is re-written using a large pulse of voltage (about 10V) that is stored up over time in a charge pump, which is both power-hungry and time consuming. Additionally the current pulse physically degrades the Flash cells, which means Flash can only be written to some fixed number of times before it must be replaced.

In contrast, MRAM requires only slightly more power to write than read, and no change in the voltage, eliminating the need for a charge pump. This leads to much faster operation, lower power consumption, and no effective "lifetime". There are no cycle limitations on the number of times users can read/write to MRAM unlike Flash or FRAM and the bits can be programmed faster than Flash. Hence it is expected that Flash will be the first memory type to eventually be replaced by MRAM.

The only current memory technology that easily competes with MRAM in terms of speed is Static RAM (SRAM).

MRAM has similar speeds to SRAM, similar density but much lower power consumption than DRAM, and is much faster and suffers no degradation over time in comparison to Flash memory. It is this combination of features that make MRAM a potential contender for the traditional memories 'replacement.

Another advantage of MRAM is that it is made of radiation hardened materials and thus finds a big market potential in military and aerospace applications.

C. Market Barriers

Getting the cost structure and the volumes for MRAMs to the point where it can have a huge impact on giant markets is still a challenge; this is a generic challenge with any new memory technology.

While MRAM as a technology has been around for several years, it has failed to achieve major commercial success for two main reasons - MRAM's uncompetitive cost per bit and the difficulty in integrating the technology into standard CMOS processes.

Freescale has addressed the cost issue with the use of an innovative MRAM cell structure incorporating what it calls a "toggle" bit, which stabilizes a cell in either the one or the zero state without requiring additional control transistors, thereby offering an optimized bit cell solution.

The process integration issue was addressed by incorporating the MRAM module late in the process flow in order to minimize any effect on the standard CMOS logic processing.

According to Freescale, technically, the biggest obstacle facing MRAM is that it takes a lot of current to switch the magnetic polarization of a cell. Thus, overly large driver transistors are necessary for writing. Reducing the large programming current and scaling down the driver transistors are a few remaining challenges in realizing the commercial potential of MRAM.

NVE Corp. was recently granted a patent on Magnetothermal MRAM which uses a combination of ultra-fast magnetic fields and heat pulses, both from electrical current, to reduce the energy required to write data and allow reduction of the memory cell size while maintaining thermal stability. Thus magnetothermal MRAM could be the MRAM of future as it promises to reduce both cell size and write current.

Initially MRAM seemed likely to emerge as the major memory solution for advanced mobile devices since it could offer the speed and capacity that would be necessary for pervasive computing applications. However the related high costs act as a deterrent and MRAM backers hope that this limitation would disappear once volume shipments were achieved.

PRAM, in contrast, is relatively easy and cheap to make. While it did face power consumption and stability issues in 2004, it later became apparent that this problem was not intrinsic to PRAM. Given the inherent limitations of today's Li-Io battery technology, heavy power consumption is equally worrisome in today's mobile environment. Both Hitachi and Philips have announced R&D-level successes in improving the power consumption characteristics of PRAM. And, with regard to the stability issues, researchers have now shown that under reasonable conditions, PRAM can demonstrate the 10-year retention rate that is expected from non-volatile memory. Thus PRAM has been shown to be much more competitive with MRAM for the crucial mobile memory space than might have been suspected a couple of years ago.

In addition, PRAM has strong backing from major industry players including Intel which sees PRAM as the most promising non volatile memory alternative, more than

MRAM. This is based on its scaling path, declining cost basis and the fact that it is bit-alterable.

D. Market Strategy

With nanotechnology enabled memory market estimated to grow to 7 B$ in 2010, most of the major players are hedging their bets on multiple technologies.

Projected by some to become a 1.5 B$ industry by 2010, almost all the tech companies have a hand in MRAM and most seem to centre around one small but crucial player, NVE Corp.

NVE has an impressive IP portfolio that includes the basic patents required for a wide range of commercial MRAM applications. As per a recent announcement, it has dropped out of the MRAM products space and will focus on MRAM only as a part of its IP portfolio.

Others like Freescale have the strategy of having MRAM as commercial products. Freescale has very recently moved a 4Mbit MRAM into volume production. In the long haul, Freescale thinks MRAM can challenge flash at the advanced nodes.

The real short-term value of Freescale's technology lies not in standalone memory replacement, where the competition over cost-per-bit is extreme, but as a key element in System-on-Chip (SOC) designs.

As an SOC element, Freescale's technology can be used to incorporate sufficiently high-density memory onto highly integrated processing units and can be leveraged into solutions by Freescale and with licensing arrangements by others.

According to the International Technology Roadmap for Semiconductors, today's SoC designs use up to 50 percent of their die area on embedded memory, normally SRAM. This figure is expected to surpass 70 percent in the not-too- distant future. While one can not discount the validity of the standalone memory potential of Freescale's MRAM product, its present pricing structure and relatively low density will keep it limited to niche applications, like battery- backed SRAMs, and for controlling mission-critical backup systems where its cumulative advantages of high performance, endurance and non-volatility make it a compelling alternative to today's high-priced solutions. Also with most of the present systems needing Flash plus SRAM which requires a continuous movement of power intensive operations back and forth, replacing these multiple configurations with MRAM will enhance performance at a cost savings.

IBM sees MRAM as a replacement for embedded DRAM.

The other strategy direction is on target applications.

While most of the players are targeting SRAM and battery backed-up SRAMs being replaced by MRAM, there is one player, Micromem, who is targeting its products at the RFID market as the first replacement for MRAM. There is no doubt that RFID is in need of a viable non-volatile memory solution and if Micromem can reach its

objective it would find itself with a large addressable market for its products/technology.

With MRAM replacing Flash, Freescale's focus will be towards the mobile market. With its strong ties to Motorola, and early entry into the MRAM business, it is believed that Freescale will help give MRAM credibility in the cell phone sector.