VLSI Design Essentials

Synopsis

This course is aimed to provide an opportunity for the participant to acquire comprehensive technical and industry relevant insight into the VLSI IC Design arena.

This course will provide a basic understanding & a holistic view of the complete VLSI chip design flow. It will enable the participant to understand the basics involved in various phases of IC design with an appreciation of the links and dependencies across them. Industry insights shared in this training help the participant appreciate the IC design flow in a real working world.

The course is structured into modules. Short interactive workshops within the course facilitate in making this an interesting, interactive learning experience. Participants will be exposed to issues cited from real industry experience. This course will be delivered by a senior VLSI consultant with extensive exposure in supporting & managing IC projects on a global scale.

What You Will Learn

After going through this training program, the participant would have learnt

- Different aspects and phases of the complete IC design flow
- These include
  - ✓ Basics of design library
  - ✓ Logic simulation and synthesis
  - ✓ Floor plan, Place & Route, Design for Manufacturability
  - ✓ Design Verification, Design for Testability
  - ✓ IPs and their usage
  - ✓ Low power design methodologies
  - ✓ Economics involved in IC design, Multi-project and Multi-wafer service
- Dependencies and links across various design phases – this, in turn, will facilitate him in comprehending how decisions made in one phase affects the other
- Be ready to handle details of each design phase

Who Should Attend

- IC design engineers with 1-3 years' experience

(*The course level is customized accordingly*)

Prerequisite

Basic engineering know how. 1-2 years' experience in IC design/support is preferable.

Course Methodology

This course is conducted in a seminar room. The course will include brief interactive workshops like sessions to encourage participation and facilitate learning. Each participant will receive a set of course material. There are no lab sessions.

Course Duration

4 days (9am – 5.00 pm)

Course Instructor

Meenu Sarin
Director, VLSI Consultancy
Tel: +65 98629814, Email: meenu@asic-vlsi.com,
Website: www.asic-vlsi.com Blog: www.asic-vlsi.com/blog
Twitter: @meenusarin Facebook: VLSI Consultancy
LinkedIn: http://sg.linkedin.com/in/meenusarin

Ms. Meenu Sarin is a microelectronics professional with over 21 years' experience in the microelectronics industry across various facets of operations & across geographies like Europe, India, Singapore, Greater China and Australia and with special focus in the semi-custom ASIC environment. She has registered her company, VLSI Consultancy, in Singapore from where she consults offering techno-commercial services to the semiconductor industry. She has conducted in-house training courses and public workshops in various countries including Singapore, Malaysia, Hong Kong and India besides delivering talks in universities. She is also a founding member and an Executive Board Member of the Singapore Semiconductor Industry Association (www.ssia.org.sg)

From 1997-2002, Meenu was a Technical Marketing Manager in STMicroelectronics (STM)/Singapore with focus on Telecom segment. In this role, she was responsible for Business Development and Program Management for STM's semicustom ASIC projects in Asia Pacific. Meenu also worked as a Program Manager in charge of managing various semi-custom projects with customers in the Asia-Pacific Region. Before her move to STM Singapore, Meenu worked at STM India from 1991 to 1997. As a Design Manager for Library Design Group, she was responsible for growing and managing a 30 member strong team involved in design and development of semi-custom digital libraries in various technologies across different platforms as per the market requirements and to support designers in STM's worldwide locations. Prior to this, Meenu had been a Design Engineer for digital library design and development at STM Italy for several years after she received her engineering degree (Computer Engineering) from Delhi Institute of Technology, India in 1988.

Course Structure

The course is organized into modules to facilitate participants to attend a specific module(s) as per their interest/need. To extract maximum benefit from the course however, participation in all modules is recommended.

A. Introduction and Design Library

1. Introduction

- Basics of IC Design Flow
- Some definitions
- Generic Technology Aspects & Trends
- Some emerging design methodologies

2. Design Library

- Definition, Library Architecture
  (With basic introduction to SSIs, IOs, Memories, IPs; general circuits used like Flip flops, latches, combinational circuits, RAMs, ROMs etc. will be included)
- Library Cell Representations
- Cell views (logical description, timing information, derating data, capacitance information, power and area information)

- Global views (max capacitance, interconnect info, max power and derating information)
- Library Characterization
  (Standard load, trip points, parasitic caps, input slew rate, timing equation, delay calculation, Voltage based and Current State models)
- Library Validation
- Trends in Library architecture
  (Power, speed optimization, drive, contents changing with technology and trends)

B. Logic Simulation & Synthesis

1. Logic Simulation

- Simulation modes (behavioral, functional, static timing analysis, gate level simulation)
- Net capacitance
- Cell model (primitive, library, macro/IP) and test bench
- SDF in simulation
- Limitations of logic simulation
- STA (STA in design flow, providing constraints for STA)

2. Logic Synthesis

- Logic synthesis in the design flow
- HDL and Synthesis – inferring logic and some HDL guidelines
- Optimization, setting constraints, operating conditions
- Handling Delays
- Memory Synthesis
- Timing driven synthesis

C. Floorplan, Placement & Routing, Finishing and DFM

1. Floorplan, Placement & Routing, Finishing

Floorplan

- Goal, objective
- Hierarchical Design
- I/O and Power planning
- Core limited and pad limited design
- Clock Planning
- Grouping and Regioning

Placement & Routing, Finishing

- Goals & Objectives
- Timing driven placement/Physical Design flow
- Information formats
- Routing (Global & detailed routing, clock routing, power routing)
- Back Annotation, Circuit extraction
- Design checks, Mask preparation

2. **DFM**
   - Need for DFM
   - Yield categories
   - Yield Optimization (Critical Area Analysis, Chemical Mechanical Polishing, Lithography Compliance Check)

D. Verification, DFT

- Need for Verification
- Functional Verification
  (Simulation, Formal Verification, Coverage – Code, Functional, Assertion)
- Timing Verification – STA, SSTA
- Physical Verification – DRC, LVS, Parasitic Extraction
- Design For Test (DFT)
  Scan (Full scan, boundary scan)
  Faults – Fault models, Fault collapsing, IDDQ test and Fault simulation
  ATPG, At speed test
  BIST (LFSR, Signature Analysis)
  Test logic insertion

E. Design for Re-use & IPs

- What is IP, what is Design Re-use
- IPs (Driving factors, Issues in IP market, P selection, Hard and soft IPs along with some guidelines, IP verification, issues arising in integrating IPs in SoC, generic portfolio)
- Concurrently developed in-house IPs
- Practical Design Re-use approach and essentials
- IP market landscape
- Industry bodies

F. Low Power Design Guidelines

- Sources of power dissipation (Static, Short circuit, dynamic)
- Power distribution considerations (Temperature, package, Voltage drop, Electromigration)
- Low power design techniques and methodologies (levels of low power optimization, includes, MSV, MTCMOS, VTCMOS, encoding, logic reduction, clock gating etc.)
- Guidelines for low power design

G. Multi Project Wafer Service/Multi Reticle Service & Economics involved and some Generics

a. Multi Project Wafer Service/Multi Reticle Service

- What is MPW
- When to/Why/Who goes for MPW
- Generic MPW Flow model
- What is Multi Reticle Service
- Foundry Perspective (Project Scheduling, Capacity Planning, General Pricing considerations)

b. Economics involved and some Generics

- Basic Economics involved in IC development
- Generic issues seen during IC implementation